## REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated May 10, 2006 (U.S. Patent Office Paper No. 04282006). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1, 4-5, 8-18 stand for consideration in this application, wherein claims 2, 3, 6 and 7 are being canceled without prejudice or disclaimer, while claims 1, 4-5, 8-9, 11-13, 16, and 18 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention.

All amendments to the application are fully supported therein. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

35 U.S.C. §102(e) rejection

Claims 13, 15, and 16-17 were rejected under 35 U.S.C. §102(e) as being anticipated by Stiffler et al. (US Pat. No. 6,622, 263). Applicants respectfully traverse the rejection of claims 13, 15, and 16-17 for the reasons set forth below.

According to the M.P.E.P. §2131, a claim is anticipated under 35 U.S.C. §102 (a), (b), and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Claim 13

Claim 13 now recites that a method for sharing an I/O device connected to a PCI bus of a computer among a plurality of virtual machines formed on a control program of said computer, comprises the steps of: selecting at most one virtual machine among said plurality of virtual machines at a time; enabling said I/O device to set a state of logical connection between said selected virtual machine and a single port of said I/O device connected to said PCI bus through said single port; and changing said state of logical connection between said

port and said selected virtual machine according to a control signal received from said selected virtual machine.

In other words, where an error occurs in the selected virtual machine, the non-selected virtual machine, in which an error does not occur, accesses the I/O device via a single port. Furthermore, since the I/O device has only a single port, non-selected virtual machine automatically cannot access the I/O device, because normal virtual machine already occupies the single port to connect to the I/O device.

In contrast, Stiffler merely describes that the storage devices are duplicated with all disk stores initiated on the primary computer echoed by the secondary computer, and maintaining synchronization between separate secondary storage devices on the two computers is relatively straightforward since all the data that is to be stored must necessarily be transferred from the primary computer to the secondary computer during the processing of each checkpoint anyway (col. 9, lines 52-61) This means that where the disk array is not dual ported, each of the primary computer and the secondary computer has the secondary storage devices in each of them as a backup and the data in the secondary storage has to be accessed to continue the operation after a fault occurs in the primary computer. This scheme is completely different from that recited in claim 13. Furthermore, Stiffler states that the disk array has to be dual ported to both the primary computer and the secondary computer, otherwise (col. 9, lines 54-56)

Therefore, Stiffler does not show every element as now recited in claim 13. Accordingly, claim 13 is not anticipated by Stiffler.

Claim 16

Claim 16 has substantially the same features as those of claim 16, particularly with respect to the I/O device being single ported and at most one selected physical partitioned computer accessing the I/O device via the single port of the I/O device. As such, the arguments set forth above are equally applicable here. Claim 13 being allowable, claim 16 must also be allowable.

Claim 15 and 17

As to dependent claims 15 and 17, the arguments set forth above with respect to independent claims 13 and 16 are equally applicable here. The base claim being allowable, claims 15 and 17 must also be allowable.

The First 35 U.S.C. §103(a) rejection

Claims 1, 3, 5 and 7 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Stiffler in view of Pittelkow et al. (US Pat. 7,003,688). As mentioned above, claims 3 and 7 are being cancelled, and therefore the rejections of claims 3 and 7 are moot. The rejection of claims 1 and 5 is respectfully traversed for the reasons set forth below.

According to the Manual of Patent Examining Procedure (M.P.E.P. §2143):

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both not found in the prior art, not in the applicant's disclosure.

Claim 1

Claim 1 recites that a computer system comprises a plurality of virtual machines formed on a control program of a computer; and an I/O device connected to a PCI bus of said computer and shared among said plurality of virtual machines; a single port disposed in said I/O device and connected to said PCI bus; PCI connection allocating means for setting a state of logical connection between selected at most one of said plurality of virtual machines and said port at a time; and I/O device switching means for updating said state of logical connection set by said PCI connection allocating means according to a control signal received from said selected virtual machine, wherein said selected virtual machine changes its state of logical connection to said I/O device according to the setting by said PCI connection allocating means, wherein said virtual machine is deactivated to said control program in response to an error occurs in said virtual machine, and wherein said control program notifies a connection destination standby-system server of said state of connection.

As set forth above, Stiffler does not show elements recited in claim 1, particularly with respect to the I/O device being single ported and at most one selected virtual machine accessing the I/P device via the single port of the I/O device.

Pittelkow does not show the elements that Stiffler fails to show. Furthermore, Pittelkow merely shows that each of the interfaces are connected through respective fibre channel media to switch which is connected to plural servers and a resource manager is notified of the failure of an interface, and then determines what targets were owned by the failed interfaces and reassigns those targets to one of the remaining interfaces. In other words, Pittelkow merely shows reallocation of the interfaces to servers in the event that the failure occurs in one of the interfaces. However, Pittelkow does not show that the virtual machine itself is deactivated to the control program in response to occurrence of an error in the virtual machine, and the control program notifies a connection destination standby server of the state of connection.

Furthermore, there is no suggestion or motivation in either Stiffler or Pittelkow to combine these features explicitly or implicitly, or in the knowledge generally available to one of ordinary skill in the art at the time the invention was made to embody all the features of the invention as recited in claim 1. Accordingly, claim 1 is not obvious in view of all the prior art.

Claim 5

Claim 5 has substantially the same features as those of claim 1, particularly with respect to the I/O device being single ported and at most one selected physical partitioned computer accessing the I/O device via the single port of the I/O device. As such, the arguments set forth above are equally applicable here. Claim 1 being allowable, claim 5 must also be allowable.

The Second 35 U.S.C. §103(a) rejection

Claims 2, 4, 6 and 8 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Stiffler in view of Pittelkow and in further view of "Computer Input/Output." Claims 2 and 6 are being canceled, and therefore the rejection of claims 2 and 6 are moot. The rejection of claims 4 and 8 is respectfully traversed for the reasons set forth below.

Claim 4

Claim 4 recites that the computer system according to claim 1, wherein said plurality of virtual machine comprise first and second virtual machines, wherein said second virtual

machine, when an error is detected in said first virtual machine, sends a predetermined control signal to said I/O device switching means and connects the port of said I/O device to said second virtual machine, and wherein said control program activates said second virtual machine and lets said first virtual machine stand by.

First, as set forth above, the combination of Stiffler and Pittelkow does not show every element as now recited in claim 1 and 5, upon which claims 4 and 8 depend. "Computer Input/Output" says nothing about the elements that Stiffler and Pittelkow fail to show.

Furthermore, the present invention recited in claim 4 does not require an additional line for sending an interruption signal. In contrast, the Examiner alleges that "Computer Input/Output" teaches the interrupt Driven I/O, wherein the I/O module (I/O device) interrupts the CPU; the CPU (computer) finishes executing the current instruction; the CPU acknowledges the interrupt; the CPU saves its current state; and the CPU jumps to a sequence of instructions which will handle the interrupt. However, the combination of Stiffler, Pittelkow, and "Computer Input/Output" requires an additional interruption signal line because a controller of Pittelkow only switches an interface with another interface in the event that failure occurs in the interface without sending an additional interruption signal to the computer.

Therefore, there is no motivation or suggestion in either Stiffler, Pittelkow or "Computer Input/Output" to combine these features explicitly or implicitly, or in the knowledge generally available to one of ordinary skill in the art at the time the invention was made to embody all the features of the invention as recited in claim 1.

Accordingly, claim 4 is not obvious over the prior art.

Claim 8

Claim 8 has the substantially same features as those of claim 4. As such, the arguments set forth above are equally applicable here. Claim 4 being allowable, claim 8 must also be allowable.

The Third 35 U.S.C. §103(a) rejection

Claims 9-12 and 14, and 18 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Stiffler in view of "Computer Input/Output." This rejection is respectfully traversed for the reasons set forth below.

As set forth above, the combination of Stiffler and "Computer Input/Output" does not embody all the features of the invention as recited in claim 9.

Claims 10-11, 14 and 18 have substantially the same features as those of claim 9, particularly with respect to the I/O device being single ported and at most one selected virtual machine accessing the I/O device via the single port of the I/O device. As such, the arguments set forth above are equally applicable here. Claim 9 being allowable, claims 10-11, 14 and 18 must also be allowable.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

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